Abstract of the Disclosure

Power consumption on programmable logic devices can be minimized by taking account of gate leakage effects. A logic design system may analyze a logic design to determine which signals are most often high and which signals are low. A logic designer may also provide information on signals to the logic design system. The logic design system may include a gate leakage optimizer and other computer-aided design tools to produce configuration data for programmable logic devices. The programmable logic device may have logic gates formed from stacks of transistors. The configuration data may be used to configure the programmable logic devices so that signals that are usually high are routed to transistors that are high in the stacks, thereby reducing gate leakage and power consumption while maintaining satisfactory performance for the device.